REMARKS

In the office action, the examiner rejected Claims 1-8 under 35 U.S.C. 102(b) as being anticipated by Watanabe (U.S. Patent No. 6,226,230). Accordingly, the applicant has amended the claims to more clearly define the essential features, thereby differentiating the present invention clearly from the prior art. More specifically, the applicant has amended Claim 1 to include the feature of "wherein the load data switching means divides the timing memory into a plurality of memory regions either in a column direction or a row direction to generate the plurality of timing data at the same time" This feature is supported by the original disclosure of the present application, for example, at page 10, lines 12-23, which reads as follows:

> According to the semiconductor test device comprising the timing generation circuit of the present invention constituted in this manner, as to the timing data stored in the timing memory, the memory region of the timing memory in which predetermined timing data is stored is divided in an address direction (memory column direction) or data bit width direction (memory row direction) by the timing generation circuit according to the present invention. Moreover, the divided timing data are combined, and acquired as the timing data indicating a predetermined delay amount or timing set number, and a pulse signal indicating a desired timing is output.

The present invention is related to a timing generation circuit and semiconductor test device having the timing generation circuit. More specifically, the present invention divides the memory area of a timing memory into an address direction or a data bit width direction. The data generated from the divided memory areas are combined to create the timing data which is expressed by two or more times larger bits of data word. Further, the data

generated from the divided memory areas are able to provide a two or more times larger number of timing sets for the timing generator. The combined timing data or the timing sets are used to generate a timing pulse signal which defines a timing edge of the test signal applied to a device under test (DUT).

The timing generation circuit under the present invention includes a timing memory (TMM) 10 which contains predetermined timing data. An address selection circuit 40 specifies two or more addresses of the timing memory TMM in response to a mode switching signal and outputting two more timing data corresponding to the two or more addresses at the same time. See, page 16, line 12 to line 25, which reads: "Moreover, a memory region of this TMM 10 can be divided by load data switching means described later. As shown in FIG. 2(b), the timing data is linked in a data bit width direction, and data having a large delay amount can be loaded as one timing data in the down counter 20 of the next stage."

The cited Watanabe reference discloses a timing signal generating apparatus that automatically detects erroneous set state. In the case where set values for defining a rising timing and a falling timing of a test pattern signal are erroneously set in a test program so as to generate a test pattern signal having its pulse duration shorter than a predetermined pulse duration, such set error can be detected by the first set error detecting apparatus and the second set error detecting apparatus. As seen from the block diagram of Figures 1 and 14, the address data of the timing memory 113C is supplied from the address counter 113D

through the single set of data bus at all times. The address counter 113D simply produces the address data by incrementing the address data in synchronism with the clock (test period). Such a relationship between the address counter 113D and the pattern (delay data) memory 113C is described from column 2, line 58 to column 3, line 3, which reads as follows:

> The delay data memory 113C is accessed by an address signal supplied from an address counter 113D. The address counter 113D generates, from the test starting time, an address signal the address of which is incremented by +1 in every test period TS_{RAT} (refer to FIG. 13). Therefore, the delay data memory 113C is accessed, in every test period TS_{RAT} during the test, by the address signal the address of which is incremented by +1 in the sequential order, and the delay data DY_S and DY_R set therein in advance are read out therefrom in every test period TS_{RAT}. Those delay data DY_S and DY_R are set in the clock generators 113A and 113B, respectively, and the set pulse P_S and the reset pulse P_R are generated based on those delay data, respectively.

Namely, there is no indication that two or more different address data are applied to the pattern memory 113C of the cited Watanabe reference. What is shown by the cited Watanabe reference is to access the pattern memory 113C by one address data which is produced by sequentially incrementing the previous address data with the clock period. Therefore, it is not possible to divide the timing memory into two or more memory regions. Consequently, it is not possible generate two or more timing data at the same time from the divided memory regions.

By combining or liking the two or more timing data retrieved from the two or more memory regions, the combined timing data is able to express the timing of much longer than that expressed by the timing data retrieved from the single memory region. In the

present invention, the mode using the combined timing data is called a long delay mode (see page 21) and the mode using the ordinary timing data is called a standard mode (see page 19). The long delay mode and the standard delay mode are switched with one another by the mode switching signal. The cited Watanabe reference does not show any idea of standard delay mode and long delay mode or the switching therebetween.

Claim 1 stand rejected for the reason that Watanabe reference shows delay data that is divided into integer portion and fraction portion. However, this division procedure is not equivalent or similar to the procedure under the present invention where the timing memory is divided into a plurality of memory regions. The division of the delay data into integer and fraction portions in the cited Watanabe reference is done by adding the delay data from the timing (delay data) memory 113C and the fixed skew value from the fixed value storage 31 and dividing the added data into the integer portion and the fraction portion. Both the summing operation and the division operation are conducted by the summation processing device 30 as shown from column 3, line 62 to column 4, line 9, which reads as follows:

> The summation processing device 30 performs an operation process for dividing a delay data by a time duration of one period of the reference clock REFCLK, and for separating the division result into an integer quotient (hereinafter referred to as an integer value) and a residue (hereinafter referred to as odd value or fraction value). The summation processing device 30 sums a delay data DY.sub.S read out from the delay data memory 113C and a fixed value skew SKEW read out from the fixed value storage device 31, and divides the summed result by a time duration of one period of the reference clock REFCLK to obtain an integer value VDAT and an odd value MDAT.

The obtained integer value VDAT is supplied to a data input terminal D of the down-counter 11, and the odd value MDAT is supplied to a data input terminal D of the first latch circuit 12.

In other words, the summation processing device 30 does not at all divide the timing memory 113C but divide the summed data into the integer portion and the fraction portion. In this configuration, the bit length of the data is always the same, i.e., there is no distinction between the standard delay mode and the long delay mode of the present invention.

As discussed above, since the essential features of the present invention are not shown or suggested by the cited Watanabe reference, the rejection under 35 U.S.C. 102(b) is no longer applicable to the present invention.

In this opportunity, the applicant has amended the abstract and specification to correct the minor wording errors therein and more clearly describe the invention. This is to verify that no new matter has been introduced by this amendment.

Under the circumstances, the applicant respectfully requests that the present application be allowed and passed to issue.

Respectfully submitted,

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